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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/950,026	09/10/2001	Manh Hung Pham	016295.0693	1709

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EXAMINER
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WILSON, YOLANDA L

ART UNIT	PAPER NUMBER
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2113

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 09/950,026	<b>Applicant(s)</b> PHAM, MANH HUNG	
	<b>Examiner</b> Yolanda L. Wilson	<b>Art Unit</b> 2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 13 February 2008.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-3,5-9,11,12,14-19,21-25,27,28 and 30-32 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3,5-9,11,12,14-19,21-25,27,28 and 30-32 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1,3,6-9,11,12,15-17,19,22-25,27,28,31,32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raynham et al. (USPN 5774647A) in view of Dearth et al. (USPN 5588112A) in view of Labatte et al. (USPN 6125392A) in view of Larson et al. (USPN 6601183B1) in further view of Wikipedia (BIOS Interrupt Call). As per claims 1 and 17, Raynham et al. discloses analyzing said memory error, determining a memory module in which said error occurred and creating a log; and storing said log in said non-volatile memory section of said memory module in column 10, lines 4-18 and the abstract. Raynham et al. discloses a BIOS in column 7, lines 55-60.

Raynham et al. fails to explicitly state wherein the log includes information identifying the cause of said error. Raynham et al. discloses that the errors are logged according to correctable and non-correctable errors.

Dearth et al. discloses this limitation in column 15, lines 9-19.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the log include information identifying the cause of said error. A person of ordinary skill in the art would have been motivated to have the log include information identifying the cause of said error because identifying the cause

of the error allows a user to determine during which operation performed by the memory the error occurred.

Raynham et al. and Dearth et al. fail to explicitly state wherein one or more BIOS routines are operable to perform the steps of creating a log and storing said log.

Labatte et al. discloses this limitation in column 1, lines 13-18.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have one or more BIOS routines be operable to perform the steps of creating a log and storing said log. A person of ordinary skill in the art would have been motivated to have one or more BIOS routines be operable to perform the steps of creating a log and storing said log because the BIOS controls the initial operations before the operating system is initiated and detects errors during initialization, see Fish et al. (20020073353A1) page 2, paragraph 0020.

Raynham et al., Dearth et al., and Labatte et al. fail to explicitly state detecting a memory error with means operable to generate an exception within said central processing unit wherein said central processing unit has an assigned exception vector.

Larson et al. discloses this limitation in column 2, line 61 – column 3, line 6.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have detecting a memory error with means operable to generate an exception within said central processing unit wherein said central processing unit has an assigned exception vector. A person of ordinary skill in the art would have been motivated to have detecting a memory error with means operable to generate an exception within said central processing unit wherein said central

processing unit has an assigned exception vector because generating an exception in response to a memory is a way of handling memory errors detected in a computer system.

Raynham et al., Dearth et al., Labatte et al., and Larson et al. fail to explicitly state associated with the assigned exception vector.

Wikipedia discloses this limitation on pages 1-3.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have associated with the assigned exception vector. A person of ordinary skill in the art would have been motivated to have associated with the assigned exception vector because the BIOS is known to be associated with interrupts to be called after certain events occur and in response actions are taken, as indicated in Larson et al. in column 2, line 61 – column 3, line 6 and Labatte et al. in column 1, lines 13-18. Also, please see Wikipedia (Interrupt descriptor table).

3. As per claims 3 and 19, Raynham et al. discloses wherein said memory error is detected during normal operation in the abstract.

4. As per claims 6,15,22,31, Raynham et al. discloses wherein said log comprises information about the date and time when said error occurred in the abstract.

5. As per claims 7 and 23, Raynham et al. discloses wherein said log comprises information about the system identification in column 7, lines 62-67.

6. As per claims 8 and 24, Raynham et al. discloses wherein said log is stored in a cyclical manner in column 10, lines 19-38.

7. As per claims 9 and 25, Raynham et al. discloses a central processing unit; a memory system coupled with said central processing unit comprising a plurality of memory module slots for receiving of memory modules, said memory module comprising a random access memory section and a non-volatile memory section; means for generating a log about said error; and means for storing said log in said non-volatile memory section of a memory module in Figure 2, abstract, in column 10, lines 4-18. Raynham et al. discloses a BIOS in column 7, lines 55-60.

Raynham et al. fails to explicitly state wherein the log includes information identifying the cause of said error. Raynham et al. discloses that the errors are logged according to correctable and non-correctable errors.

Dearth et al. discloses this limitation in column 15, lines 9-19.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the log include information identifying the cause of said error. A person of ordinary skill in the art would have been motivated to have the log include information identifying the cause of said error because identifying the cause of the error allows a user to determine during which operation performed by the memory the error occurred.

Raynham et al. and Dearth et al. fail to explicitly state wherein BIOS routines are operable to perform the steps of creating a log and storing said log.

Labatte et al. discloses this limitation in column 1, lines 13-18.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have BIOS routines be operable to perform the steps of

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creating a log and storing said log. A person of ordinary skill in the art would have been motivated to have BIOS routines be operable to perform the steps of creating a log and storing said log because the BIOS controls the initial operations before the operating system is initiated and detects errors during initialization, see Fish et al.

(20020073353A1) page 2, paragraph 0020.

Raynham et al., Dearth et al., and Labatte et al. fail to explicitly state means for detecting an error in said memory system wherein said means for detecting an error generate an exception within said central processing unit wherein said central processing unit has an assigned exception vector.

Larson et al. discloses this limitation in column 2, line 61 – column 3, line 6.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have means for detecting an error in said memory system wherein said means for detecting an error generate an exception within said central processing unit wherein said central processing unit has an assigned exception vector. A person of ordinary skill in the art would have been motivated to have means for detecting an error in said memory system wherein said means for detecting an error generate an exception within said central processing unit wherein said central processing unit has an assigned exception vector because generating an exception in response to a memory is a way of handling memory errors detected in a computer system.

Raynham et al., Dearth et al., Labatte et al., and Larson et al. fail to explicitly state associated with the assigned exception vector.

Wikipedia discloses this limitation on pages 1-3.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have associated with the assigned exception vector. A person of ordinary skill in the art would have been motivated to have associated with the assigned exception vector because the BIOS is known to be associated with interrupts to be called after certain events occur and in response actions are taken, as indicated in Larson et al. in column 2, line 61 – column 3, line 6 and Labatte et al. in column 1, lines 13-18. Also, please see Wikipedia (Interrupt descriptor table).

8. As per claims 11 and 27, Raynham et al. discloses wherein said non-volatile memory is divided in a plurality of sub sections each sub section storing one log in column 10, lines 19-31.

9. As per claims 12 and 28, Raynham et al. discloses wherein said sub sections are written in a cyclical manner in column 10, lines 19-31.

10. As per claims 16 and 32, Raynham et al. discloses wherein said log comprises information about the system identification in column 7, lines 62-67.

### ***Claim Rejections - 35 USC § 103***

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claims 2,5,14,18,21,30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raynham et al. in view of Dearth et al. in view of Labatte et al. in



view of Wikipedia (BIOS Interrupt Call) in further view of Brisse et al. (WO 99/05599).

As per claims 2 and 18, Raynham et al., Dearth et al., and Labatte et al. fail to explicitly state wherein said memory error is detected during a diagnostic test.

Brisse et al. discloses this limitation on pages 8 and 9, 'In another embodiment of the invention, memory errors may be detected during manufacture...This embodiment may be utilized in manufacturing test images and systems undergoing hot room testing.'

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have said memory error is detected during a diagnostic test. A person of ordinary skill in the art would have been motivated to have said memory error is detected during a diagnostic test because memory errors occur during test and are logged to indicate which memory locations have erred.

13. As per claims 5,14,21,30, Raynham et al., Dearth et al., and Labatte et al. fail to explicitly state wherein said log comprises information about the location of the memory module.

Brisse et al. discloses this limitation on page 7, "Once the actual slot number of the interface slot with the error is determined, then the process continues to step 310 in which the actual slot number is stored in the Windows NT<sup>TM</sup> system registry."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have said log comprises information about the location of the memory module. A person of ordinary skill in the art would have been motivated to have said log comprises information about the location of the memory module because the slot id which indicates the location of the memory module within the system

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is used to determine the memory module with the error. Brisse et al. discloses this on page 7, "As is known in the art, the system registry is a system database maintained by the operating system to store data such as, for example...information relating to installed hardware and software devices. In preferred embodiments, the driver 2 increments an error count in the system registry. Upon detection of an error, the driver 2 preferably reports such error and count to the well known Windows NT™ System Event Log..."

### ***Response to Arguments***

14. Applicant's arguments with respect to claims 1-3,5-9,11,12,14-19,21-25,27,28,30-32 have been considered but are moot in view of the new ground(s) of rejection. In view of the amendments made to the claims, a reference has been found to reject the newly added limitation to the independent claims. Please see the above rejection.

### ***Conclusion***

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

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shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda L. Wilson whose telephone number is (571) 272-3653. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Yolanda L Wilson/  
Primary Examiner, Art Unit 2113